19. (Twice Amended) A method of inspecting a semiconductor device, comprising the steps of:

positioning the semiconductor device as defined in claim 13 by using the end parts as the positioning references; and

inspecting electrical characteristics of the semiconductor device.

C6

20. (Twice Amended) A method of mounting a semiconductor device comprising the steps of:

positioning the semiconductor device as defined in claim 13 by using the end parts as the positioning references; and

mounting the semiconductor device on a circuit board.

REMARKS

Claims 1-20 are pending. By this Amendment, claims 1-4, 7, 10, 13, 19 and 20 are amended.

The attached Appendix includes a marked-up copy of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance for the reasons discussed herein; (b) do not raise any new issue requiring further search and/or consideration since the amendments amplify issues previously discussed throughout prosecution; (c) satisfy a requirement of form asserted in the previous Office Action; (d) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (e) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

I. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1, 2 and 4-20 under 35 U.S.C. §103(a) over U.S. Patent No. 5,117,282 to Salatino. This rejection is respectfully traversed.

The invention of claims 1 and 13 include a second portion positioned between end parts of a first portion. For example, see in Fig. 2, the second portion 16 between the end parts, each of which may be a portion of the projected section 18.

Salatino fails to disclose the second portion positioned between the end parts of the first portion.

II. Conclusion

In view of the foregoing, Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Michael Britton
Registration No. 47,260

JAO:MB/djb

Attachment:
Appendix

Date: February 19, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Twice Amended) An interconnect substrate over which an interconnect pattern is formed, comprising:

a first portion; and

a second portion to be superposed on the first portion,

wherein the first portion has ~~an~~ end parts as ~~a~~ positioning references; and

wherein the second portion has a shape so as to be superposed on and inside the first portion except the end parts, the second portion positioned between the end parts.

2. (Amended) The interconnect substrate as defined in claim 1,

wherein each of the end parts as the positioning references includes two edges which are perpendicular to each other.

3. (Amended) The interconnect substrate as defined in claim 1,

wherein the first portion comprises a rectangular body section and a projected section which extends from at least one edge of the body section and includes one of the end parts.

4. (Amended) The interconnect substrate as defined in claim 3,

wherein the projected section is a region determined by:

an edge which is a boundary between the projected section and the body section;

a first edge which is perpendicular to the edge as a boundary; and

a second top edge which is parallel to the edge as a boundary,

wherein one of the end parts as ~~a~~ the positioning references includes the first and second edges.

7. (Amended) The interconnect substrate as defined in claim 6,

~~wherein the first portion has a plurality of the end parts as positioning references; and~~

wherein at least one of the end parts is formed from an area in the body section other than an area from which the projected section extends.

10. (Twice Amended) The interconnect substrate as defined in claim ~~7~~1, wherein a plurality of holes are formed in the end parts.

13. (Twice Amended) A semiconductor device comprising:

at least one semiconductor chip; and

a substrate which has a first portion and a second portion to be superposed on the first portion, and on which the semiconductor chip is mounted,

wherein the first portion includes ~~an~~ end parts as ~~a~~ positioning references; and

wherein the second portion has a shape so as to be superposed inside the first portion and avoid being superposed over the end parts of the first portion, the second portion positioned between the end parts.

19. (Twice Amended) A method of inspecting a semiconductor device, comprising the steps of:

positioning the semiconductor device as defined in claim 13 by using ~~a plurality of~~ the end parts as the positioning references; and

inspecting electrical characteristics of the semiconductor device.

20. (Twice Amended) A method of mounting a semiconductor device comprising the steps of:

positioning the semiconductor device as defined in claim 13 by using ~~a plurality of~~ the end parts as the positioning references; and

mounting the semiconductor device on a circuit board.